SAMSUNG ELECTRONICS

A comprehensive assessment of EUV mask defect printability

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Challenges in Defect Inspection for EUVL

How can we detect smaller defect than today?

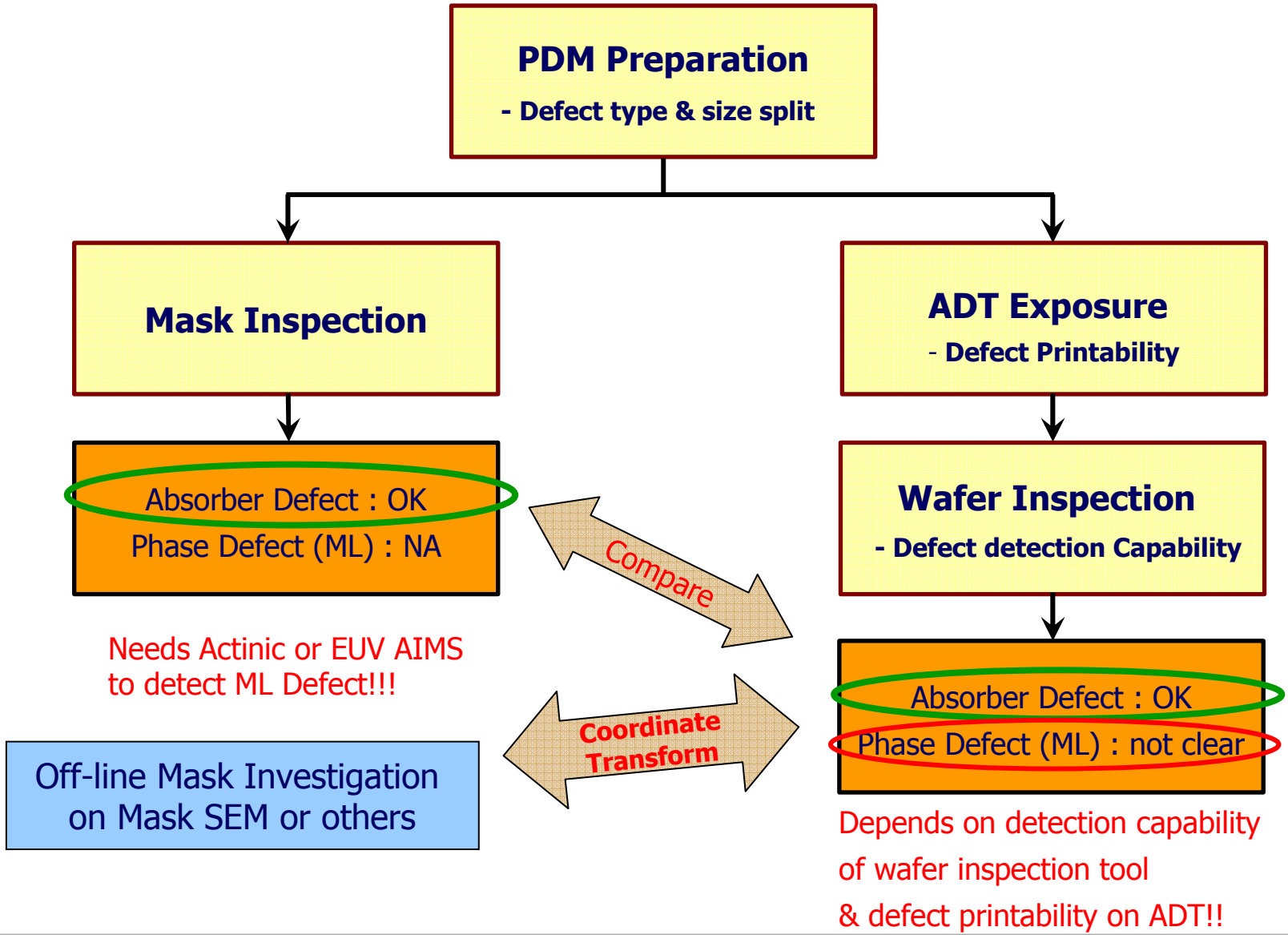
- As design rule gets smaller, detection of smaller defects become critical.

Phase defect detection in EUVL.

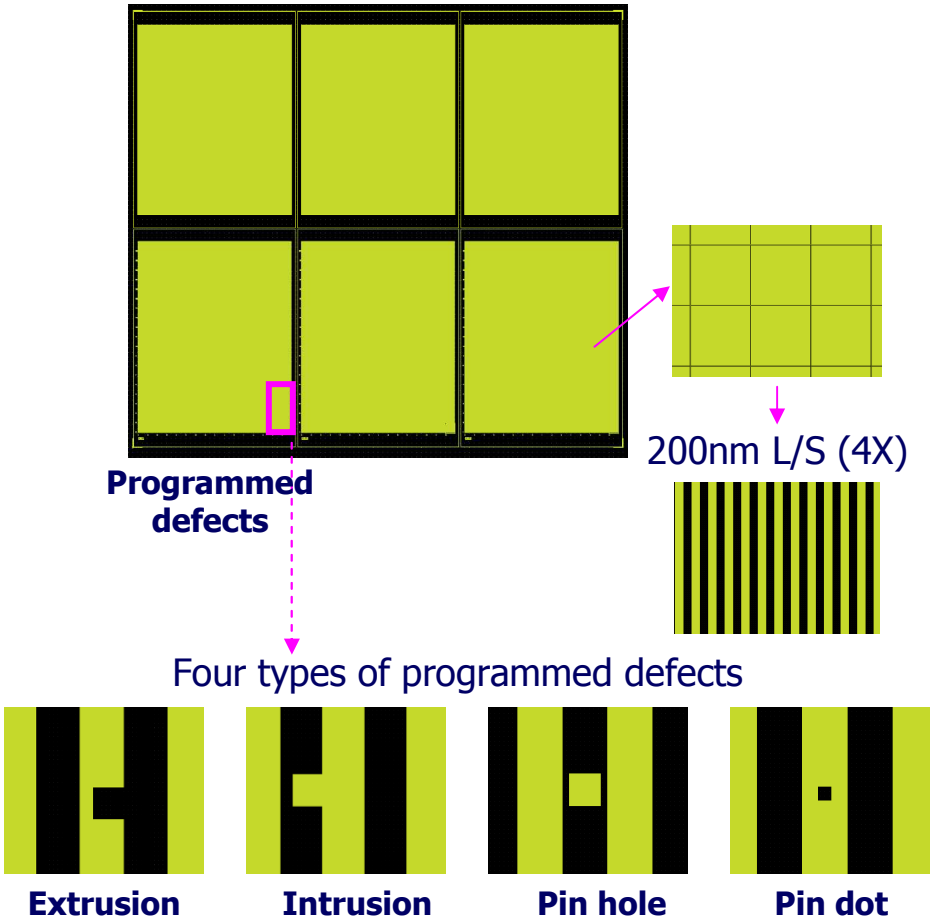
- EUV AIMS tool may not be available till 2012
- What can be done during EUV R&D phase?
  - Detection of phase defect on wafer level
  - Defect review & analysis of Mask and wafer level result

Need optimization of defect inspection procedure on wafer level.
Which is the optimized wafer stack for best signal?
How many defects are on the mask?

Defect Inspection Assessment for EUVL

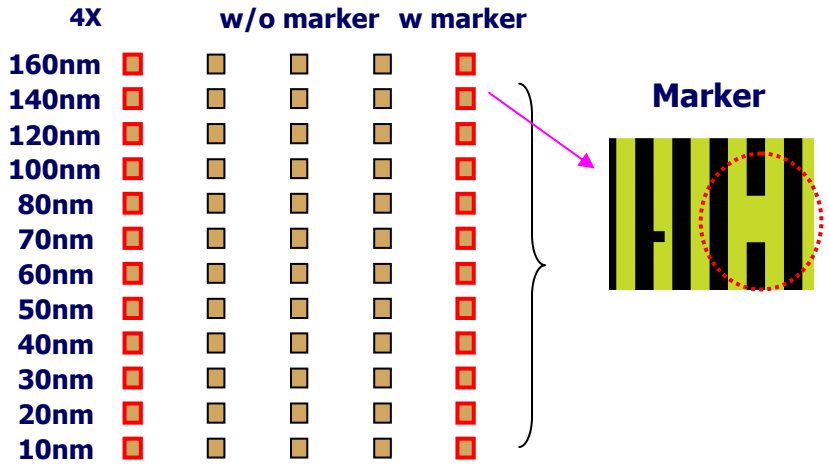


Mask Layout Description & experimental conditions



Experimental condition

- Wafer stack : Oxide or SiN
- Film thickness : 120nm/80nm, on underlayer
- Exposure : Conventional NA0.25 σ0.5 @ EUV
  Alpha Demo Tool (ADT), IMEC
- Wafer Inspection tool : KLA 28XX
  Patterned Mask Inspection tool : KLA5XX

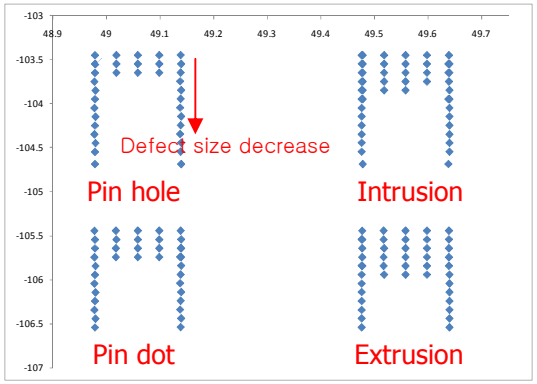


Defect detection sensitivity

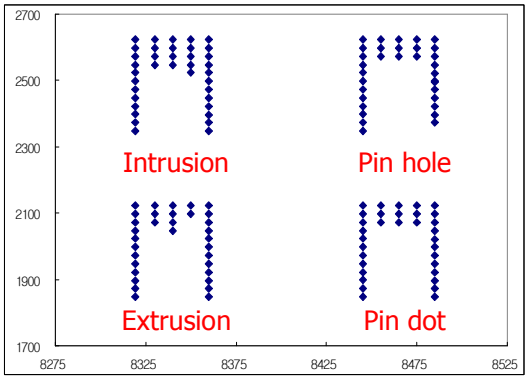
PDM1 inspection results for PD (programmed defect)

- Oxide + P1101, ADI/ACI inspection results @ IMEC
- SiN + SEVR40, ADI/ACI inspection results @ SEMATECH

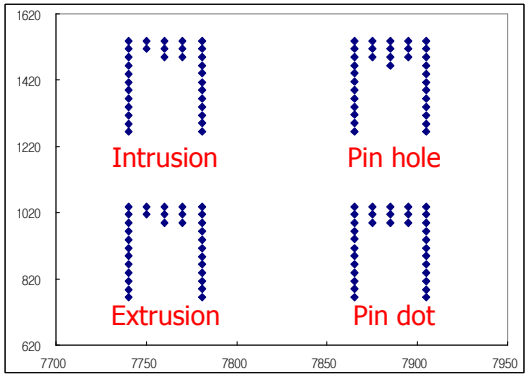
Mask inspection



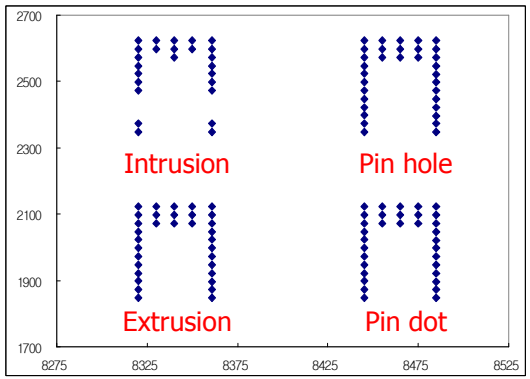
Wafer Inspection (ACI-SiN)



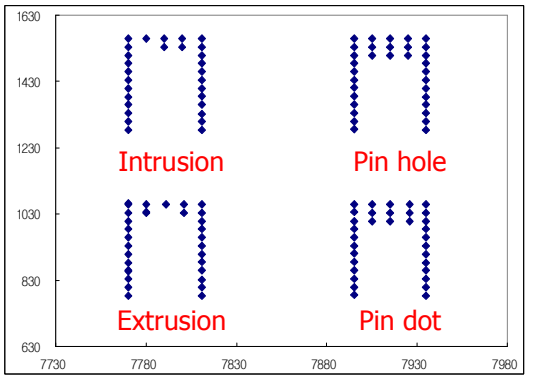
Wafer Inspection (ACI - Oxide)



Wafer Inspection (ADI - SiN)



Wafer Inspection (ADI - PEOX)



Defect detection sensitivity

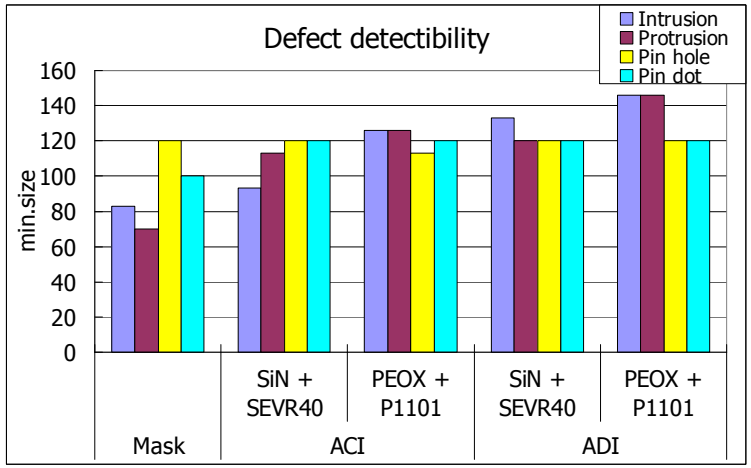
ΔCD/CDref @ ADI

100% >50% <50% 0%

In	140	120	100	80	70	60
Oxide	0.48	0.28	0.16	0.13	0.14	-
SiN	0.37	0.31	0.16	0.12	0.11	0.05
Ex	140	120	100	80	70	60
Oxide	-	0.52	0.21	0.20		0.08
SiN	-	0.36	0.18	0.12		0.05
Hole	140	120	100	80	70	60
Oxide	-	-	0.18	0.06	0.10	0.11
SiN	-	-	0.13	0.04	0.03	0.03
Dot(S)	140	120	100	80	70	60
Oxide	-	-	0.07	0.05	0.05	
SiN	-	-	0.13	0.05	0.03	0.04

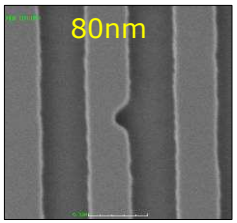
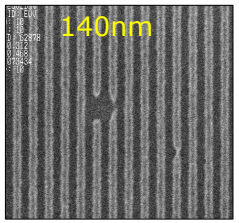
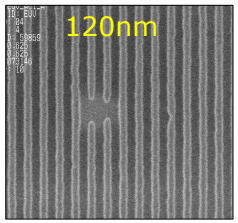
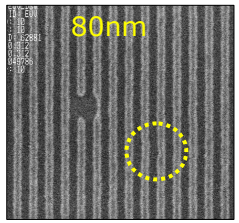
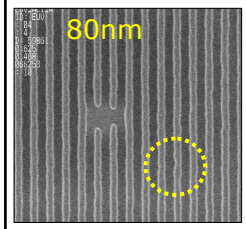
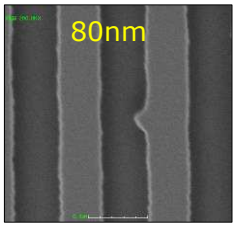
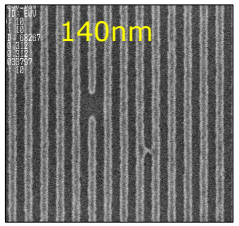
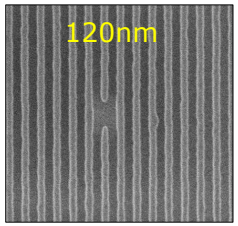
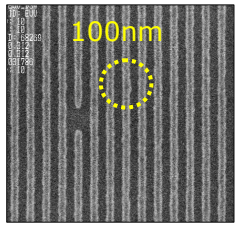
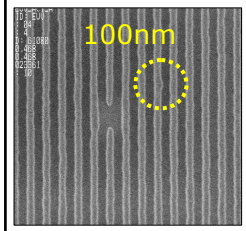
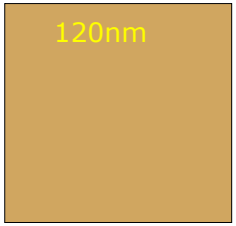
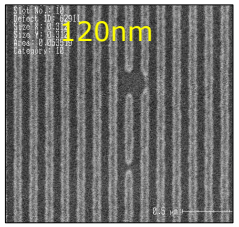
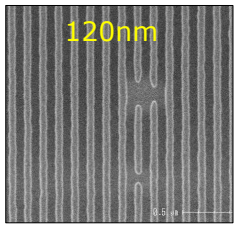
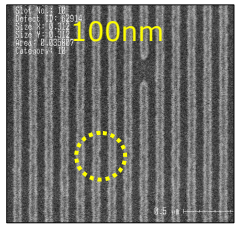
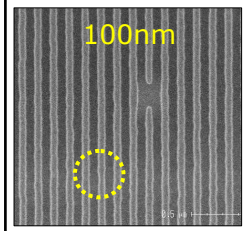
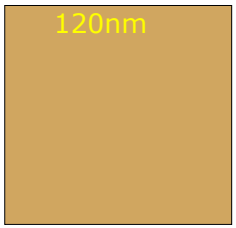
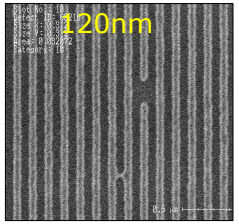
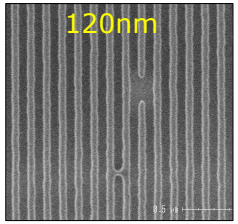
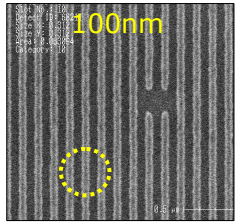
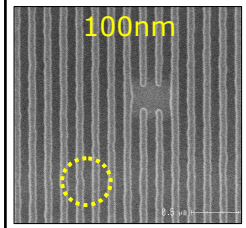
ΔCD/CDref @ ACI

In	140	120	100	80	70	60
Oxide	-	0.27	0.19	0.11	0.2	0.08
SiN	-	0.37	0.14	0.09	0.13	0.03
Ex	140	120	100	80	70	60
PEOX	-	0.35	0.16	0.08	-	0.05
SiN(270)	0.45	0.33	0.21	0.09	-	0.04
Hole	140	120	100	80	70	60
Oxide	-	-	0.12	0.09	0.05	0.04
SiN	-	-	0.15	0.05	0.03	-
Dot(S)	140	120	100	80	70	60
Oxide	-	-	0.13	0.01	0.03	0.03
SiN	-	-	0.12	0.04	0.01	0.01



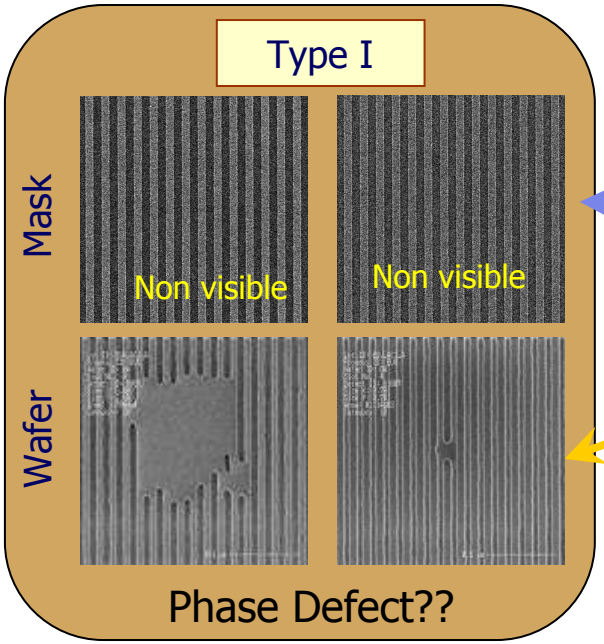
- Mask inspection tool can detect the smallest defect.
- ACI inspection > ADI inspection.
- SiN stack wafer > Oxide stack wafer.
- **Best wafer inspection result till date**
  - ➔ **SiN stack wafer at ACI.**

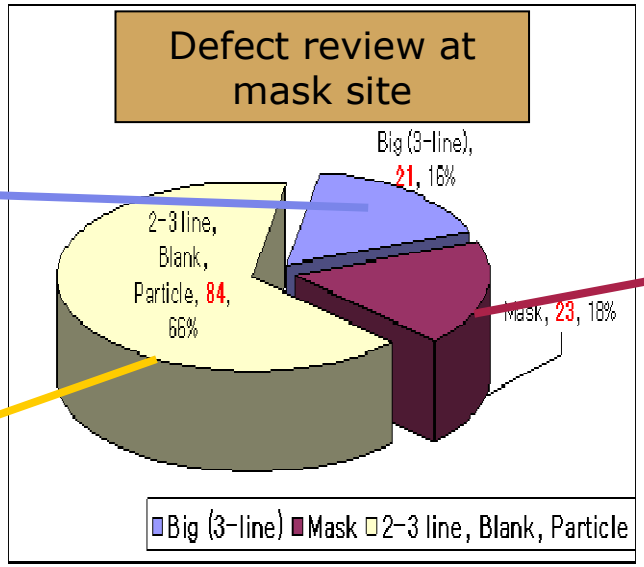
Defect Printability vs Detectability

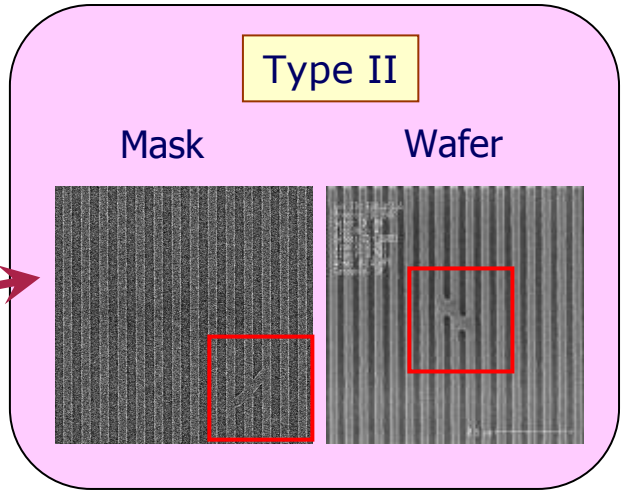
X4	Mask	ADI KLA	ACI KLA	Print.(ADI)	Print.(ACI)
Intrusion					
Extrusion					
Pin hole					
Pin dot					

Mask Inspection Capability ≥ Defect printability@ ADT

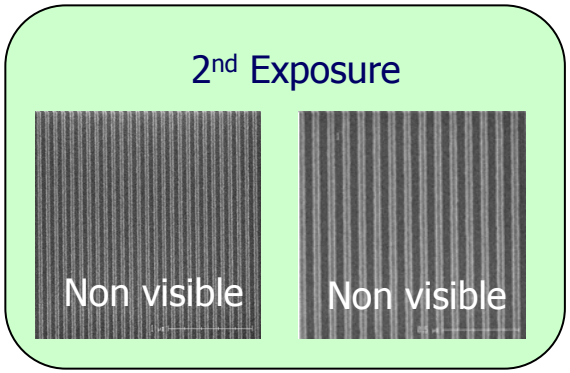
Phase Defect Trace







Mask Cleaning

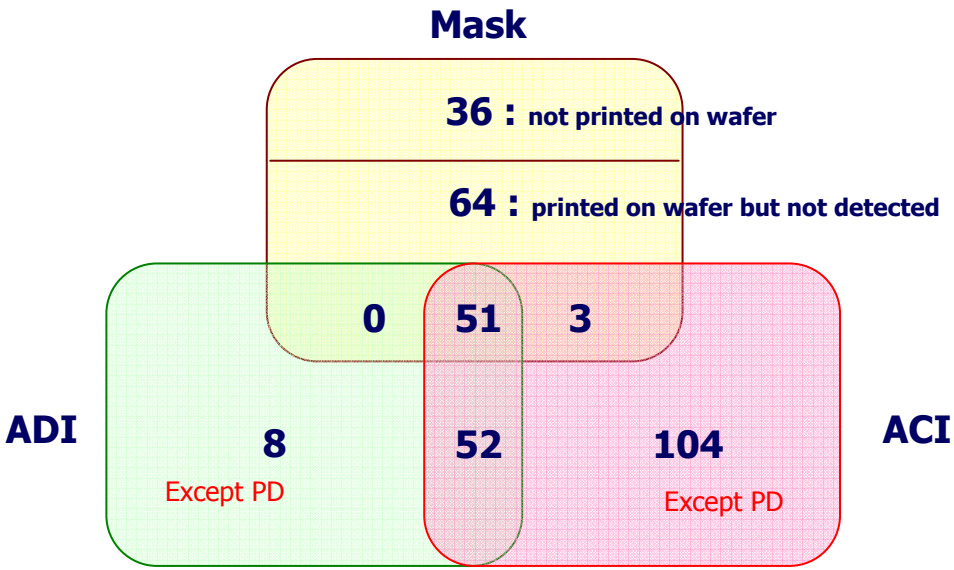


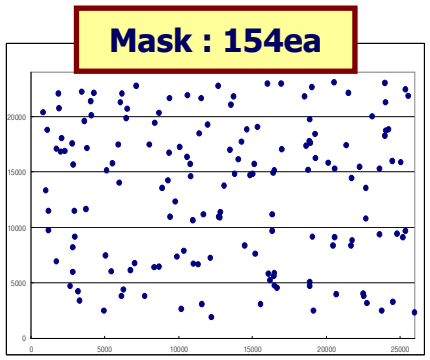
- Are Type I defects, phase defects?
- Type I defects were not found at the same position after: Mask cleaning → Expose → review.
- Therefore, the source of type I defects seems to be from mask handling (moving particles?).

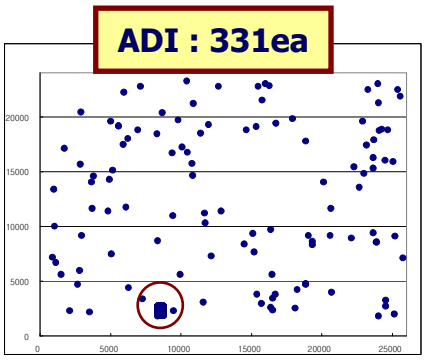
Defect Inspection Results

PDM2, 50nm HP L/S

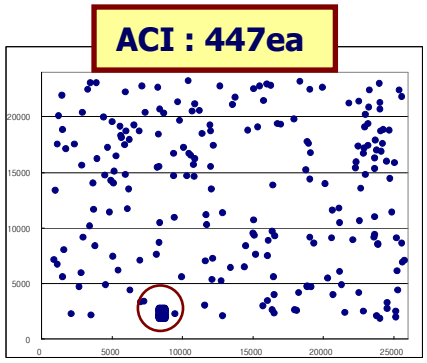
- SiN + SEVR40, mask/ADI/ACI inspection results @ SEMATECH





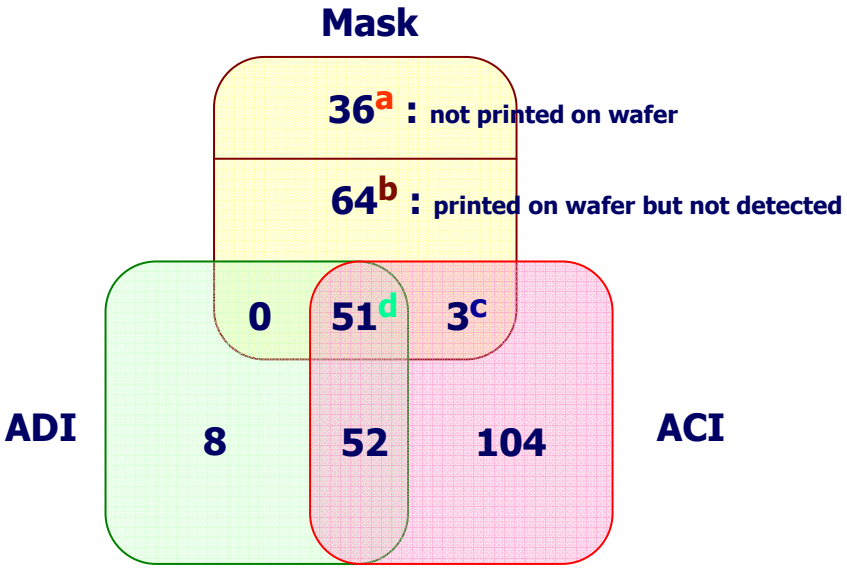


Programmed defect area

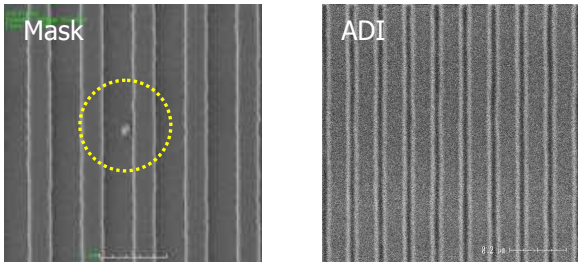


Programmed defect area

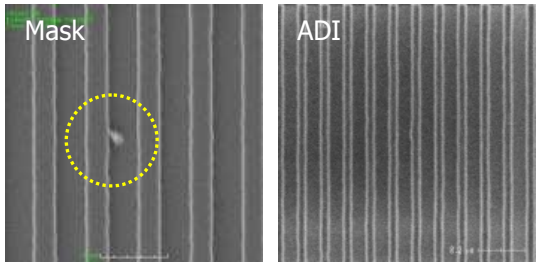
Defect Analysis – Mask



a. Detected by Mask inspection tool but not printed on wafer → 36 small defects

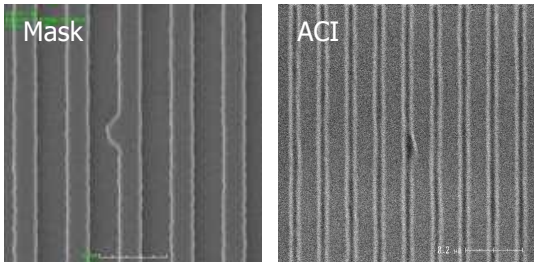


b. Detected by Mask inspection tool and printed on the wafer → 64 small defects



Mask inspection tool can detect smaller defects.

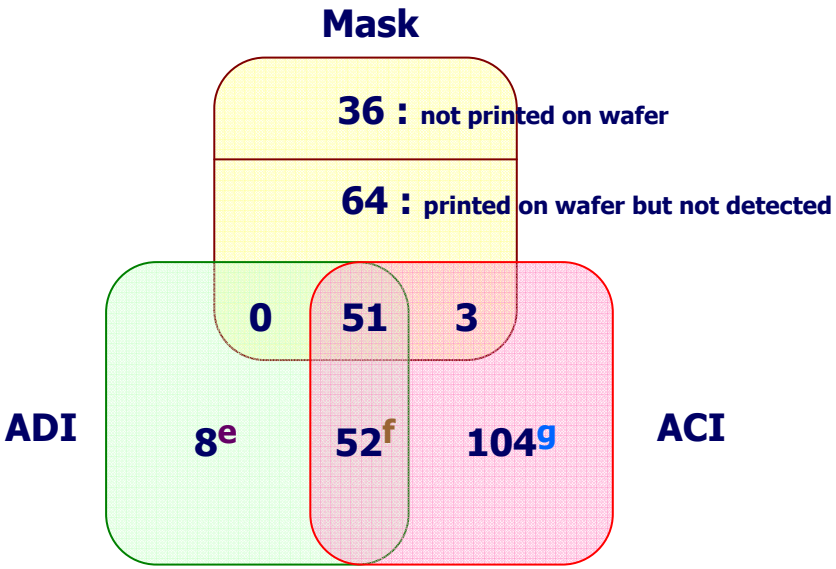
c. Mask ∩ ACI → 3 small defects



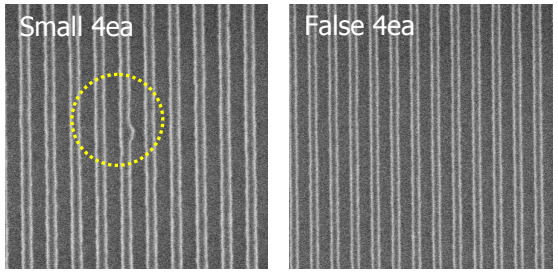
d. Mask ∩ ACI ∩ ADI → 51 defects
Extrusion, multi-line bridge, etc

Detectability of smaller defects at ACI is better than at ADI.

Defect Analysis – ADI & ACI



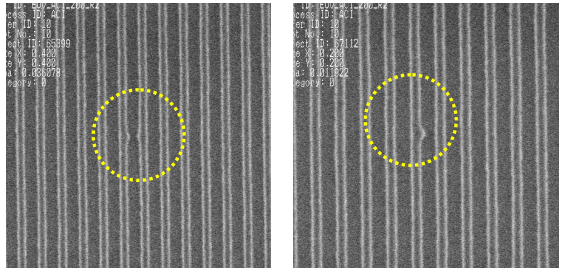
e. Only ADI → 4 small defects + 4 false



f. ADI ∩ ACI → 52 defects

protrusion	23
2 lines bridge	27
3 lines bridge	0
big	1
Notching	1

g. Only ACI → 28 small defects & remaining-false



ACI inspection can detect smaller defect than ADI

Total 84 defects (= 52 + 4 (of e,8) + 28 (of g,104)) are most probably phase defect.
More inspection required.

Summary

- Size of printable defect on wafer > 80nm(4x).

  Mask inspection tool can detect defects of sizes: 80~120nm(4X).

  Wafer inspection tool can detect defects > 120nm(4X).

- Detection capability :

  Mask inspection > ACI inspection > ADI inspection.

  SiN wafer with low LWR resist > Oxide wafer with high LWR resist.

  Further investigations needed with wafer stacks with higher S/N ratio.

- Reliable detection of smaller defects is critical for continuous downscaling of design rule. It is of paramount importance to control defects in order to successfully implement EUV Lithography.

  Requires development of highly sensitive wafer inspection tool.

- As shown in this presentation, a number of defects that were previously suspected to be phase defects, are removed by a simple mask cleaning. These defects predominantly arise during mask handling. Therefore mask handling is a critical challenge.

Acknowledgement

We appreciate the efforts for defect study to

- IMEC EUV Team
- ASML EUV Support Team
- SEMATECH EUV Team
- Samsung Mask Shop EUV Team
- Samsung R&D Etch Group